CMOS Process Photodiode Memory

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Abstract— Demand for high-speed dynamic reconfiguration of a programmable device is increasing for raising the performance level of such devices. To support high-speed dynamic reconfiguration, optically reconfigurable gate arrays (ORGAs) have been developed. An ORGA consists of a holographic memory, a laser array, and an optically reconfigurable gate array VLSI. The holographic memory can store many configuration contexts. Moreover, its large-bandwidth optical connection enables high-speed reconfiguration.Nevertheless,in previously proposed ORGA-VLSIs,the static configuration memory to store a single configuration context consumed a large implementation area of the ORGA-VLSIs and prevented the realization of large-gate-count ORGA-VLSIs. Therefore, a CMOS process photodiode memory has been newly fabricated to increase the gate density of ORGAs. The photodiode memory uses the junction capacitance of photodiodes as dynamic memory, thereby obviating the static configuration memory.

Index Terms— CMOS, Dyanamic Optically Reconfigurable Gate Array, FPGA, Holographic Memory, Optically Reconfigurable Logic Block, Optically Reconfigurable Switching Matrix

1 INTRODUCTION

All computer systems produced today use reduced instruction set computer (RISC) architectures [1],[2]. Such architectures are beneficial in terms of higher clock frequency, smaller implementation area, and lower power consumption than conventional complex instruction set computer (CISC) architectures [3][4]. Those various benefits derive from an extremely straight forward principle: the simplest circuit is the best. The simplest circuit can operate at the highest clock frequency, in the smallest implementation area, and with the lowest power consumption because the simplest circuit can be constructed with fewer selector passes, less load capacitance of short metal wires. This principle of simplicity is also applicable to programmable devices. Ultimately, the simplest processor type on a programmable device in a single instruction set computer that includes only a single instruction [5]. Focusing on a single clock cycle, even RISC, its arithmetic logi unit (ALU) can only execute a single instruction. Even if many instructions are implemented onto the ALU, all instructions other than a single operated instruction can be regarded as superfluous instructions because the instructions are never executed. Generally, if clock-by-clock reconfiguration is possible on a programmable device, then only circuits that must be executed within a single clock cycle should be implemented onto the programmable device. A single instruction set computer can operate at the highest clock frequency, with the lowest power consumption, and in the smallest implementation area. Moreover, the smallest implementation area enables large parallel computation if the same implementation area is used as that of a conventional RISC processor. Consequently, the overall performance can be increased dramatically.

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However, to support such implementation of the single instruction set computer, high-speed dynamic reconfiguration capability is necessary for a programmable device.

Recently, field programmable gate arrays (FPGAs) have come to be used widely for various applications [6]-[8]. Moreover, an FPGA with optical communication functions have been developed [9]. However, since FPGA reconfiguration requires more than a few hundred milliseconds. FPGAs are unsuitable as dynamically reconfigurable devices.Therefore, optically reconfigurable gate arrays (ORGAs) have been developed to realize such dynamic high-speed reconfiguration [10]-[18]. An ORGA consists of holographic memory, a laser array, and an optically reconfigurable gate array VLSI. Circuit information or configuration contexts can be stored on a holographic memory. The configuration contexts can be addressed using a laser array. Finally, those contexts can be optically programmed onto an optically reconfigurable gate array. The optically reconfigurable gate array architecture realizes high-speed reconfiguration since the bandwidth of an optical bus between a holographic memory and a programmable gate array VLSI is extremely large. Moreover, numerous reconfiguration contexts can be realized since the storage capacity of a three-dimensional holographic memory is greater than that of silicon memories.

The maximum reconfiguration time of 13.75 ns has been reported [13]. Furthermore, an ORGA has achieved 144 reocnfigurable contexts [14]. Therefore, high-speed dynamic reconfiguration capabilities has been demonstrated.Nevertheless, is previously proposed ORGA-VLSIs, the static configuration memory to store a single configuration context consumed a large implementation area of the ORGA-VLSIs and prevented the realization of large-gate-count ORGA-VLSIs. Therefore, a CMOS process photodiode memory has been newly fabricated to increase the ORGA gate density. It uses the junction capacitance of photodiodes as dynamic memory, thereby obviating the static configuration memory.

II. DYANAMIC OPTICALLY RECONFIGURABLE GATE ARRAY VLSI

A new high-sensitivity optically reconfigurable gate array VLSI (ORGA-VLSI) chip was designed and fabricated using standard complementary metal oxide semiconductor (CMOS) process technology, as portrayed in Fig. 1. Transmission gates and photodiode cells were designed as custom cells with height equal to that of standard cells. The gate array design was synthesized by combining such custom cells and standard cells and using a logic synthesis tool(Design compiler).

Fig. 1. Photograph of a CMOS process high-sensitivity optically reconfigurable gate array VLSI.

Table 1. Specifications of the high-sensitivity ORGA-VLSI.

Technology	0.18 μm double-poly 5-metal CMOS process
Chip size	5.0 × 2.5 [mm]
Supply Voltage	Core 1.8V, I/O 3.3V
Photodiode size	4.40 × 4.45 [μm]
Photodiode response time	< 5 ns
Sensitivity	2.12×10^{-14} J
Distance between Photodiodes	h.=30.08, v.= 30.24 [μm]
Number of Photodiodes	10,322
Number of Logic Blocks	80
Number of Switching Matrices	90
Number of Wires in a Routing Channel	8
Number of I/O blocks	8 (32 bit)
Gate Count	2,720

Then, a place and route for the synthesized gate array design was executed using Astro (Synopsys Inc.) . Finally, the ORGA-VLSI was fabricated at a Rohm manufacturing facility. The specifications are presented in Table 1. Voltages of the core and I/O cells were designed, respectively, as 1.8 V and 3.3 V. Photodiodes were constructed between an N-well and a P-substrate. The photodiode junction area was designed as 4.40 µm× 4.45 µm. The photodiode cells are arranged at 30.08 µm horizontal intervalsand at 30.24 µm vertical intervals. This design incorporates 10,322 photodiodes. To increase the photodiode sensitivity, the photodiodes's parasitic capacitance must be decreased. Therefore, a refresh transistor and an optical amplifier connected to a photodiode were designed to be as small as possible to reduce the load capacitance and drain capacitance.

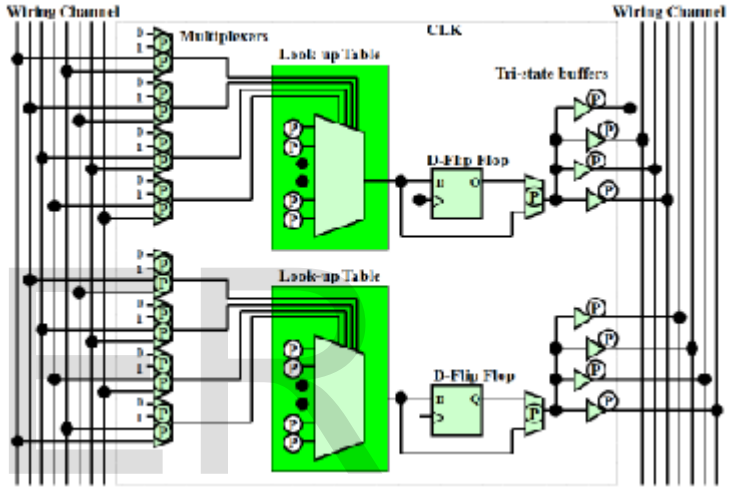

Fig. 2. Block diagram of an optically reconfigurable logic block (ORLB).

The gate array of the ORGA-VLSI uses an island style. The basic functionality of a gate array is fundamentally identical to that of currently available field programmable gate arrays (FPGAs). In all, 80 optically reconfigurable logic blocks (ORLBs), 90 optically reconfigurable switching matrices (ORSMs), and 8 opically reconfigurable I/O blocks (ORIOBs), which include 4 programmable I/O bits, were implemented in the gate array. The ORLBs, ORSMs, and ORIOBs are programmable block-by-block respectively through 69, 49 and 49 optical connections. Each block is also reconfigurable block-by-block. The total gate count is 2,720.

A.Optically reconfigurable logic block

The block diagram of an optically reconfigurable logic block is presented in Fig. 2. Each optically reconfigurable logic block consists of 2 four-input one-output look-up tables (LUTs), 10 multiplexers, 8 tri-state buffers, and 2 delay-type flip-flops with a reset function. The signals from a wiring channel connected to the optically reconfigurable logic block, which are applied through some switching matrices and/or optically reconfigurable I/O blocks, are transferred to LUTs

through eight multiplexers. The LUTs are used for implementing Boolean functions. The outputs of a LUT are connected to a multiplexer. A combinational circuit and sequential circuit can be chosen by changing the multiplexer, which is possible also in FPGAs. Finally, outputs of the multiplexer are connected to another wiring channel again through 8 tri-state buffers. In all, 69 photodiodes are used for programming an optically reconfigurable logic block. The optically reconfigurable logic block can be reconfigured perfectly in parallel. The size is 288 × 192.48 μm^2. Such an optically reconfigurable logic block design is based on a standard cell design, except for the custom designs used for the transmission gate cells and photodiode cells.

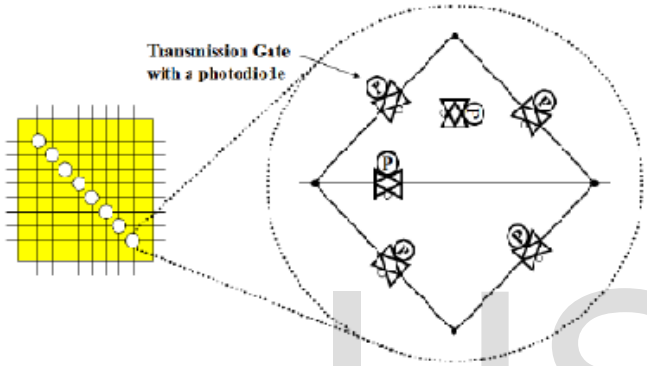

Fig. 3. Block diagram of an optically reconfigurable switching matrix.

B. Optically reconfigurable switching matrix

A block diagram of an optically reconfigurable switching matrix is portrayed in Fig. 3. Its basic construction is the same as that used by Xilinx Inc. Four-directional switching matrices with 48 transmission gates were implemented in the gate array. Each transmission gate can be regarded as a bi-directional switch. A photodiode connected to each transmission gate controls whether the transmission gate is closed or not. The four-direction switching matrices can be programmed as 49 optical connections. The cell size is 197.76 × 192.48 μm^2. Such an optically reconfigurable switching matrix was designed using custom cells of photodiode cell and transmission gate cells, except for some buffers.

III. EVALUATION

A.Calculation method of a holographic memory

Here, a thin holographic medium is introduced. An aperture plane of target lasers, a holographic plane, and an ORGA-VLSI plne are parallelized. The laser beam is assumed as a collimated beam, from which the reference wave propagates into the holographic plane. The holographic medium comprises rectangular pixels on the $x_1 - y_1$ holographic plane. The pixels are assumed as analog values. The input object comprises rectangular pixels on the $x_2 - y_2$ object plane. The pixels can be modulated to be either on or off. The intensity distributed of a holographic medium is calculable using the following equation.

$$H(x_1, y_1) \propto \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} O(x_2, y_2)\sin(kr)dx_2dy_2,$$

$$r = \sqrt{Z_L^2 + (x_1 - x_2)^2 + (y_1 - y_2)^2}$$

In that equation, $O(x_2, y_2)$ takes a binary value of a reconfiguration context, k signifies the wave number, and Z_L denotes the distance between the holographic plane and the object plane. The value $H(x_1, y_1)$ is normalized as 0-1 for the minimum intensity H_{min} and maximum intensity H_{max} , as explained in the following.

$$H'(x_1, y_1) = \frac{H(x_1, y_1) - H_{min}}{H_{max} - H_{min}}. \quad (1)$$

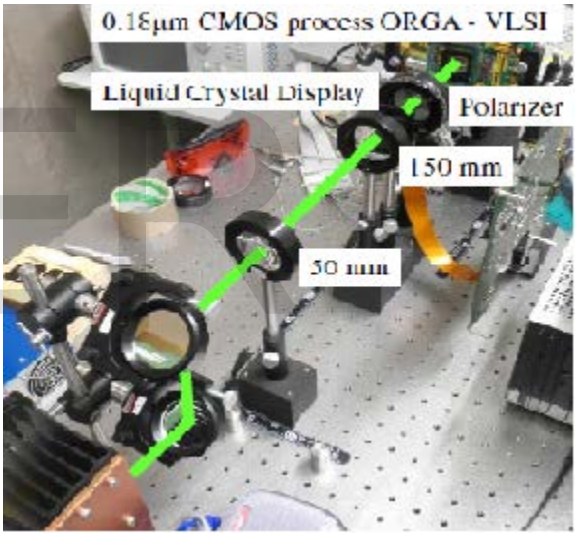

Fig. 4. Estimation system.

Finally the normalized image H' is used for implementing a holographic memory. Other areas on the holographic plane are opaque to the illumination.

B.Optical system setup

As shown in Fig. 4, an ORGA system was constructed using a liquid crystal spatial light modulator (LC-SLM) as a holographic memory and a 532 nm, 300 mW laser. The 1.7-mm-diameter beam from the laser source is expanded by three times to 5.1 mm using two lenses with 50 mm focal length. The expanded beam is incidentto the holographic memory on the LC-SLM. The LC-SLM used in this experiment is a projection TV panel, which is a 90^0 twisted nematic device with a thin film transistor. The panel consists of 1,920 × 1,080 pixels, each

having a size of 8.5 × 8.5 μm². The LC-SLM is connected to an evaluation board. The video input of the board is connected to the external display terminal of a personal computer. Programming for the LC-SLM is executed by displaying a holographic memory pattern with 256 graduation levels on the personal computer display. The ORGA-VLSI was placed 100 mm distant from the LC-SLM. The ORGA's control signals were generated using a cyclone II FPGA.

C.Experimental Results

Here, a two-bit multiplier circuit was implemented. The holographic memory pattern is shown in Fig. 5. In addition, the CCD-captured configuration context pattern, which was generated from the holographic memory pattern of Fig. 5, is shown in Fig. 6. Then the reconfiguration times and retention time of the new process ORGA was 339 ns. Results show that the new process ORGA's reconfiguration frequency or photocircuit sensitivity can be improved to 3.23 times faster than

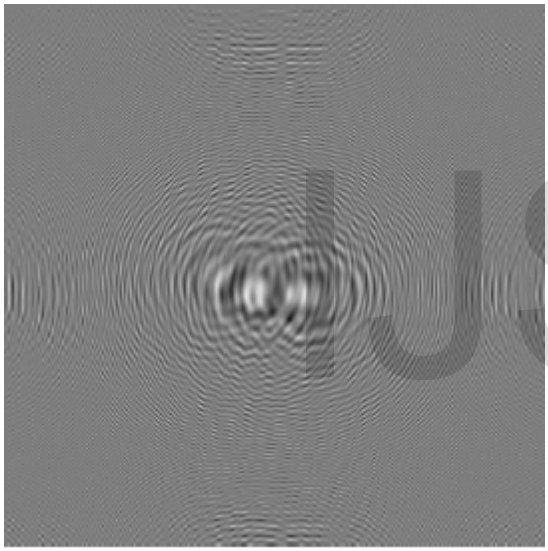

Fig. 5. Holographic memory pattern (700 × 700 pixels) including a two-bit multiplier circuit.

Fig.6. CCD-captured configuration context pattern of the two-bit multiplier circuit.

that of the conventional 0.35 μm CMOS process ORGA. In addition, the retention time of photodiode memory architecture has been measured as 2.390 ms by using a He-Ne laser's system. Compared with current DRAM, the retention time of 2.390 ms is sufficiently long to maintain the gate array state of an ORGA-VLSI .

IV. Conclusion

Currently, demand for high-speed dynamic reconfiguretion of a programmable device is continuing to increase to improve the performance of such devices. Up to the present increasingly sophisticated optically reconfigurable gate arrays (ORGAs) have been developed to support high-speed dynamic reconfiguration. Nevertheless, in previously proposed ORGA-VLSIs, the static configuration memory to store a single configuration context consumed a large implementation area of ORGA-VLSIs and prevented the realization of large-gate-count ORGA-VLSIs. Therefore, a CMOS process photodiode memory has been newly fabricated to increase the gate density of ORGAs. It uses the junction capacitance of photodiodes as dynamic memory, thereby obviating the static configuration memory. The retention time of 2.390 ms is sufficiently long to maintain the gate array state of an ORGA-VLSI.

REFERENCES

[1] Y. Pizhou, L. Chaodong, "A RISC CPU IP core," International Conference on Anti-counterfeiting, Security and Identification, pp. 356-359, 2008.
[2] J. Goodacre, A. N. Sloss, "Parallelism and the ARM instruction set architecture," Computer, Vol.38, Issue 7, pp. 42-50, 2005.
[3] T. Jami, "RISC Versus CISC," IEEE Potentials, Vol. 14, Issue 3, pp. 13-16, 1995.
[4] D. B. Tolley, "Analysis of CISC versus RISC microprocessors for FDDI network interfaces, " Conference on Local Computer Network, pp. 485-493, 1991.
[5] Y. Nihira, M, Watanabe, "Mono-instruction computer on a dynamically reconfigurable gate array," Workshop on Sysnthesis and System Integration of Mixed Information technologies, pp. 66-70, 2012.
[6]Altera Corporation, "Altera Devices," http://www. altera. com.
[7] Xilinx Inc., "Xilinx Product Data Sheets," http://www. xilinx. com.
[8] Lattice Semiconductor Corporation, "LatticeECP and EC family Data Sheet," http://www.latticesemi.co.jp/products, 2005.
[9] Prosenjit Mal, Prerna D. Patel, and Fred R. Beyette, "Design and Demonstration of a Fully Integrated Multi-Technology Applications," IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, Vol. 56, No. 6, pp. 1182-1191, 2009.
[10] J. Mumbru, G. Panotopoulos, D. Psaltis, X. An, F. Mok, S.

Ay, S. Barna, E. Fossum, "Optically Programmable Gate Array," SPIE Of Optics in Computing 2000, Vol. 4089, pp. 763-771, 2000.
[11] J. Mumbru, G. Zhou, X. An, W. Liu, G. Panotopoulos, F. Mok, and D. Psaltis, "Optical memory for computing and information processing," SPIE on Algorithms, Devices, and Systems for Optical Information Processing III, Vol. 3804, pp. 14-24, 1999.
[12] J. Mumbru, G. Zhou, S. Ay, X. An, G. Panotopoulos, F. Mok, and D. Psaltis, "Optically Reconfihurable Processors,"SPIE Critical Review 1999 Euro-American Workshop on Optoelectronic Information Processing, Vol. 74, pp. 265-288, 1999.
[13] M. Nakajima, M. Watanabe, "A13.75 ns holographic reconfiguration of an optically differential reconfigurable gate array," International Conference on Intelligent Information Hiding and Multimedia Signal Processing, pp. 852-855, 2009.
[14] Y. Yamaji, M. Watanabe, "A 144-configuration context MEMS optically reconfigurable gate array," IEEE International SOC Conference, CD-ROM, 2011.
[15] M. Watanabe, F. kobayashi, "Dynamic Optically Reconfigurable Gate Array," Japaneese Journal of Applied Physics, Vol. 45, No. 4B, pp. 3510-3515, 2006.
[16] M. Miyano, M. Watanabe, F. kobayashi, "Optically Differential Reconfigurable Gate Array," Electronics and Computers in Japan, Part II, Issue 11, vol. 90, pp.132-139, 2009.
[17] M. Watanabe, T. Shiki, F. kobayashi, "Scaling prospect of optically differential reconfigurable gate array VLSIs, " Analog Integrated Circuits and Signal Processing, Vol. 60, Issue 1-2, pp. 137-143, 2009.
[18] D. Seto, M. Nakajima, M. Watanabe, "Dynamic optically reconfigurable gate array very large-scale integration with partial reconfiguration capability," Applied Optics, Vol. 49, Iss. 36, pp. 6986-6994, 2010.
[19] M. Watanabe, F. kobayashi, "A Logic synthesis and place and route environment for ORGAs," International conference on engineering of reconfigurable systems and algorithms, pp. 237-238, 2006.